Serial No. 09/605,293
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Appendix

In the Specification

At page 8, lines 2-13 should read:

With continued reference to Fig. 1, the layer 14 of silicon dioxide 16 is formed on the substrate 12 by an conventional oxidation process or deposition process, and has been doped with hydrogen ions to provide a surface conducive to the deposition of polycrystalline silicon. Depending upon the nature of the layer 14 of silicon dioxide 16, the layer 14 of silicon dioxide 16 can be formed by thermal oxidation, chemical vapor deposition CVD), low pressure chemical vapor deposition (LPCVD), plasma enhanced chemical vapor deposition (PECVD), metalorganic chemical vapor deposition (MOCVD), and sputtering. The layer 18 of polycrystalline silicon 20 is formed on the layer 14 of silicon dioxide 16 by any deposition process currently used in the art to form a layer of polycrystalline silicon on a layer of silicon dioxide. Useful deposition methods include, but are not limited to, [thermal oxidation,] CVD, LPCVD, PECVD, MOCVD and sputtering.

At page 9, lines 17-21 should read:

After the hydrogen ions have been implanted into the layer 14 of silicon dioxide 16, the layer 18 of polycrystalline silicon 20 is formed on the layer 14. The layer 18 of polycrystalline silicon 20 is formed on the layer 14 by any deposition method currently in use in the art. Useful deposition methods include, but are not limited to, [thermal oxidation,] CVD, LPCVD, PECVD, MOCVD and sputtering.

At page 10, lines 21-28 should read:

Fig. 2 presents a cross sectional view of a field effect transistor 50 formed by the method of the present invention. The field effect transistor 50 is formed on semiconductor substrate 52[, which is desirably silicon dioxide, quartz or glass]. The field effect transistor 50 includes a gate oxide 54, a source 56 and a drain 58. The gate oxide 54, the source 56 and the drain 58 are formed in the substrate 52. A layer 64 of

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polysilicon 66 is formed on the gate oxide 54 to form a gate electrode 70. A pair of spacers 68 are formed on the sides of the layer 64 of polysilicon 66. A layer 72 of a field oxide 74 is also formed on the substrate 52.

At page 13, lines 2-9 should read:

A thin film transistor 200 is shown in cross section in [Fig. 3] Fig. 5. The thin film transistor 200 includes an insulating substrate 202. A layer 204 of a semiconducting material 206 is formed on the surface of the substrate 202. A source region 208 and a drain region 210 are formed on the layer 204 of semiconducting material 206. A layer 212 of a dielectric material 214 is formed on the layer 204 of semiconducting material 206 and covers the source 208 and the drain 210. A layer 216 of a conducting material 218 is formed on the layer 212 of dielectric material 214 to form a gate electrode 220.

At page 13, lines 17-28 should read:

After the insulating substrate 202 has been doped with hydrogen ions, the layer 204 of semiconducting material 206 is formed on the substrate 202 by any conventional deposition process. Useful deposition methods include, but are not limited to, [thermal oxidation,] CVD, LPCVD, PECVD, MOCVD and sputtering. [Desirably, the layer 204 is deposited by a thermal oxidation process.] The layer 204 of semiconducting material 206 can be any material used to form semiconducting layers, including, but are not limited to, gallium arsenide, indium phosphide, polycrystalline silicon, and germanium. Desirably, the layer 204 of semiconducting material 206 is formed form polycrystalline silicon. Once the layer 204 of semiconducting material 206 has been formed, the layer 204 is etched to isolate the various regions of semiconducting material from each other on the surface of the substrate 202.

At page 14, lines 12-18 should read:

As a final step, a layer 216 of a conducting material 218 is formed on the layer 212 of dielectric material 214. The layer 216 is formed in any manner currently used in the art to form such layers. Useful deposition methods include, but are not limited to, [thermal oxidation,] CVD, LPCVD, PECVD, MOCVD and sputtering. The conducting

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material 218 is selected from the group consisting of polycrystalline silicon, metal, and any conducting material. The layer 216 of conducting material 218 forms the gate electrode 220.

In the Claims

10. (Thrice Amended) A field effect transistor comprising:

a semiconductor substrate;

a layer of silicon dioxide formed on at least a portion of said semiconductor substrate, said layer of silicon dioxide having hydrogen ions implanted therein by plasma source ion implantation, wherein said layer of silicon dioxide is free of metal contaminants;

a layer of polycrystalline silicon formed on at least a portion of said layer of silicon dioxide, said layer of polycrystalline silicon having a smooth morphology; and

a gate oxide formed on said semiconductor substrate from said layer of silicon dioxide having hydrogen ions implanted therein by plasma source ion implantation;

a source[,] and a drain [and a gate oxide] formed in said semiconductor substrate with a gate electrode formed on said semiconductor substrate from said layer of polycrystalline silicon to form a field effect transistor.

11. (Thrice Amended) A memory array comprising:

a semiconductor substrate;

a layer of silicon dioxide formed on at least a portion of said semiconductor substrate, said layer of silicon dioxide having hydrogen ions implanted into at least a portion of said layer of silicon dioxide by plasma source ion implantation, wherein said layer of silicon dioxide is free of metal contaminants;

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a layer of polycrystalline silicon formed over at least said portion of said layer of silicon dioxide into which said hydrogen ions were implanted, said layer of polycrystalline silicon having a smooth morphology;

a plurality of memory cells arranged in rows and columns, each of said plurality of memory cells comprising at least one field effect transistor; [and]

a gate oxide for each of said field effect transistors formed on said semiconductor substrate from said layer of silicon dioxide having hydrogen ions implanted therein by plasma source ion implantation;

[a gate oxide,] a source and a drain for each of said field effect transistors formed in said semiconductor substrate; and

a gate electrode for each of said field effect transistors formed on said semiconductor substrate from said layer of polycrystalline silicon.

12. (Thrice Amended) A semiconductor wafer comprising:

a wafer including a semiconductor substrate, said wafer being divided into a plurality of die;

a layer of silicon dioxide formed on at least a portion of said semiconductor substrate, on each of said plurality of die said layer of silicon dioxide having hydrogen ions implanted into at least a portion of said layer of silicon dioxide by plasma source ion implantation, wherein said layer of silicon dioxide is free of metal contaminants;

a layer of polycrystalline silicon formed over at least said portion of said layer of silicon dioxide into which said hydrogen ions were implanted, said layer of polycrystalline silicon having a smooth morphology; [and]

a repeating series of gate oxides formed on said semiconductor substrate from said layer of silicon dioxide having hydrogen ions implanted therein by plasma source ion implantation;

a repeating series [of gate oxides,] sources and drains for at least one field effect transistor formed in each of said plurality of die, said series of gate oxides, sources and drains being formed in said semiconductor substrate; and

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a repeating series of gate electrodes for at least one field effect transistor formed on each of said plurality of die, said series of gate electrodes being formed on said semiconductor substrate from said layer of polycrystalline silicon.

14. (Thrice Amended) A thin film transistor comprising:

a semiconductor substrate formed from a material selected from the group consisting of silicon dioxide, quartz and glass, said semiconductor substrate having hydrogen ions implanted therein by plasma source ion implantation, wherein said semiconductor substrate is free of metal contaminants;

a layer of polycrystalline silicon formed on at least a portion of semiconductor substrate, said layer of polycrystalline silicon having a smooth morphology;

a layer of a insulating material formed on at least a portion of said layer of polycrystalline silicon;

a gate oxide formed on said semiconductor substrate from said layer of silicon dioxide having hydrogen ions implanted therein by plasma source ion implantation;

[a gate oxide,] a source region and a drain region formed in said layer of polycrystalline silicon; and

a gate electrode formed on said layer of insulating material.

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